Abstract

A split gate flash memory cell structure is disclosed for prevention of reverse tunneling. A gate insulator layer is formed over a semiconductor surface and a floating gate is disposed over the gate insulator layer. A floating gate insulator layer is disposed over the floating gate and sidewall insulator spacers are disposed along bottom portions of the floating gate sidewall adjacent to said gate insulator layer. The sidewall insulator spacers are formed from a spacer insulator layer that had been deposited in a manner that constitutes a minimal expenditure of an available thermal budget and etching processes used in fashioning the sidewall insulator spacers etch the spacer insulator layer faster than the gate insulator layer and the floating gate insulator layer. An intergate insulator layer is disposed over exposed portions of the gate insulator layer, the floating gate, the floating gate insulator layer and the sidewall insulator spacers. A conductive control gate is disposed over the intergate insulator layer, covering about half of the floating gate.